AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Claims 1-15 (Canceled).

16. (Currently Amended) An integrated circuit comprising:

a plurality of metal layers comprising a plurality of conductors to interconnect components in said integrated circuit, said metal layers comprising:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors developed independent from routing of conductors for circuits outside said self contained layout section in said integrated circuit; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of ~~the~~ said metal layer in said second metal layer group directly adjacent to ~~said portion of said metal layer for~~ said self contained layout section, and wherein conductors for said second metal layer group are routed independent from routing of conductors for said self contained layout section,

~~whereby~~ wherein said preferred Manhattan direction conductors of said self contained ~~layer~~ layout section within said first metal layer group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said self contained layout section conductors are deposed in either a horizontal or vertical direction; and

wherein said self contained layout section is a section less than the entire area of said metal layer in said first metal layer group.

17. (Original) The integrated circuit as set forth in claim 16, wherein said self contained layout section is independent of a layout for said second metal layer group.

18. (Currently Amended) The integrated circuit as set forth in claim 16, further comprising a plurality of self contained layout sections in said first metal layer group.

19. (Original) The integrated circuit as set forth in claim 18, wherein at least one of said self contained layout sections comprise a wiring direction perpendicular to a wiring direction of a second one of said self contained layout sections.

20. (Cancel).

21. (Original) The integrated circuit as set forth in claim 16, wherein said first metal layer group comprises three metal layers.

22. (Currently Amended) The integrated circuit as set forth in claim 21, wherein said three metal layers ~~each~~ comprise first, second, and third metal layers, each of said three metal layers comprising conductors deposed in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

23. (Original) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

24. (Original) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

25. (Currently Amended) The integrated circuit as set forth in claim 16, wherein said self contained layout section comprises a layout for a memory block.

26. (Canceled).

27. (Currently Amended) The integrated circuit as set forth in claim 16, wherein said self contained layout section comprises a section less than 10 percent of the entire area of said metal layer in said first metal layer group.

28. (Currently Amended) A method for deposing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors~~, for the portion of said metal layer,~~ developed independent from routing of conductors for circuits outside said self contained layout section in said integrated circuit; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of ~~the~~ said metal layer in said second metal layer group directly adjacent to ~~said portion of said metal layer for~~ said self contained layout section, and wherein conductors for said second metal layer group are routed independent from routing of conductors for said self contained layout section,

~~whereby~~ wherein said preferred Manhattan direction conductors of said self contained ~~layer~~ layout section within said first metal layer group do not electrically cross-couple with

conductors of said second metal layer group regardless of whether said self contained layout section conductors are deposed in either a horizontal or vertical direction; and

wherein said self-contained layout section is a section less than the entire area of said metal layer in said first metal layer group.

29. (Original) The method as set forth in claim 28, wherein said self contained layout section is independent of a layout for said second metal layer group.

30. (Currently Amended) The method as set forth in claim 28, further comprising a plurality of self contained layout sections in said first metal layer group.

31. (Original) The method as set forth in claim 30, wherein at least one of said self contained layout sections comprise a wiring direction perpendicular to a wiring direction of a second one of said self contained layout sections.

32. (Cancel).

33. (Original) The method as set forth in claim 28, wherein said first metal layer group comprises three metal layers.

34. (Currently Amended) The method as set forth in claim 33, wherein said three metal layers ~~each~~ comprise first, second, and third metal layers, each of said three metal layers comprising conductors deposed in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

35. (Original) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

36. (Original) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

37. (Currently Amended) The method as set forth in claim 28, wherein said self contained layout section comprises a layout for a memory block.

38. (Canceled).

39. (Currently Amended) The method as set forth in claim 28, wherein said self contained layout section comprises a section less than 10 percent of the entire area of said metal layer in said first metal layer group.

40. (New) An integrated circuit (IC) comprising:

a plurality of wiring layers;

a pre-designed circuit block occupying a region on said IC and having wiring on a set of at least two wiring layers, wherein all the wiring for connecting internal circuits of said pre-designed circuit block are on said set of wiring layers within said region, wherein a top wiring layer in said set of wiring layers has a first preferred direction; and

a second wiring layer that is immediately above said top wiring layer in said set of wiring layers, said second wiring layer having a second preferred direction that is neither parallel nor orthogonal to said first preferred direction in order to reduce cross-coupling between said second wiring layer and said pre-designed circuit block.

41. (New) The IC of claim 40, wherein said pre-designed circuit block is an intellectual property (IP) block.

42. (New) The IC of claim 40, wherein said pre-designed circuit block is a memory block.

43. (New) The IC of claim 40 further comprising a plurality of pre-designed circuit blocks with wiring on said set of wiring layers.

44. (New) The IC of claim 40, wherein said second preferred direction comprises a 45° angle with respect to said first preferred direction.

45. (New) The IC of claim 40, wherein said second preferred direction comprises a 60° angle with respect to said first preferred direction.

46. (New) The IC of claim 40, wherein a preferred direction is a direction for at least fifty-percent of the wires on a layer;

47. (New) The IC of claim 40 further comprising wiring not within said region to connect said pre-designed circuit block to circuits that are not within said circuit blocks.

48. (New) The IC of claim 40, said set of wiring layers comprising first, second, and third Manhattan layers, said three Manhattan layers comprising wire segments deposed in preferred Manhattan directions, wherein:

said first Manhattan layer is the top metal layer of said set of wiring layers, and comprises a third preferred Manhattan direction; and

said second Manhattan layer is below said first Manhattan layer, and comprises a fourth preferred Manhattan direction complementary to said third preferred Manhattan direction.

49. (New) The IC of claim 48, wherein said third Manhattan layer is below said second Manhattan layer, and comprises a fifth preferred Manhattan direction complementary to said fourth preferred Manhattan direction.

50. (New) The IC of claim 48, wherein said second preferred direction comprises a 45° angle with respect to said third preferred Manhattan direction.